An Improved Two-Switch Bridgeless PFC SEPIC Structure for Total Harmonic Distortion Reduction and Circulating Current Minimization

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***Abstract*—This paper presents an improved two-switch bridgeless PFC SEPIC (TSBPFC SEPIC) structure for reducing current total harmonic distortion (THD) and minimize circulating current. A conventional PFC SEPIC structure which has an integration between SEPIC and full-bridge rectifier possess some problems high current THD_i output voltage ripple and a low *PF*. The existing bridgeless PFC SEPIC structure has two input inductors (L_1 and L_2) that causes circulating current and thus producing high current THD_i at input source. In order to improve the existing structure of bridgeless PFC SEPIC, the proposed converter an additional capacitor is connected in parallel of input diode. In addition, comparisons between two converter which are existing bridgeless PFC SEPIC and Improved TSBPFC SEPIC structure are discussed. The prototype with specification of 100 W and 48 V dc output voltage is developed. The results show THD_i of 0.99% and power factor of 0.98 are achieved with 50 kHz switching frequency.**

Keywords—bridgeless PFC SEPIC, circulating current, power factor, THD_i

I. INTRODUCTION

The AC power supplies are commonly used to supply the power to the load depending on the load requirement. However, these power supplies are usually connected to the non-linear load such as electronic devices i.e., personal computer (PC), smart phone, battery charger, datacom, telecom, EV, and industrial electronic. Hence, the power quality issues at the AC grid system such as power factor, total harmonic distortion, and output voltage ripple[1]–[3] need to be considered as the equipment to obey the harmonic pollution limitation and standards, for example the IEC 61000-3-2-1 to ensure the THD_i less than 5% [4].

Generally, when an AC source supply is connected to the DC load, the integration between full-bridge rectifier and DC-DC converter will be required, thus power factor correction (PFC) need to considered. The PFC can be classified into two major categories that are based on input PFC or output PFC. The input PFC is located at the AC source side while the output PFC at the load side. For both the input and output PFC, there are two cases that need to considered that are the active PFC using active switch and passive PFC using passive component [5]–[8]. However, the integration of full-bridge rectifier with SEPIC conventional PFC SEPIC structure possess several issues such as high THD_i, presence of extra energy at the output full-bridge, low output voltage ripple, high conduction loss, high number of power converter and low *PF* [9], [10].

Back in 1983, the first bridgeless PFC boost topology is proposed by D.M. Michel [11] to reduce the conduction loss as well as to reduce number of component. However, the bridgeless PFC boost structure has drawbacks of the high start-up inrush current, the input and output isolation cannot be easily implemented, and DC output voltage is always higher than the peak input voltage as well as a lack of current limiting during overload conditions. Back in 2009, the first bridgeless PFC SEPIC topology is proposed by Esam H. Ismail [12] and has the advantages of easy application for transformer isolation, the inrush current can be restricted during start-up and overload circumstances, the input current ripple is reduced, and lower electromagnetic interference (EMI) related to the DCM topology. Furthermore, many existing bridgeless PFC SEPIC topologies have been proposed to improve the performance of the converter by low conduction loss and switching loss, of components, unity power factor, THD_i, low cost, minimized circulating current, and reduced input voltage sensing [13]–[19]. Nevertheless, all of the issues cannot be solved in one converter but only the priority issues need to be considered. Fig. 1 shows the existing bridgeless PFC SEPIC that has an advantage of using a single-switch, which easy to be controlled and less in cost.

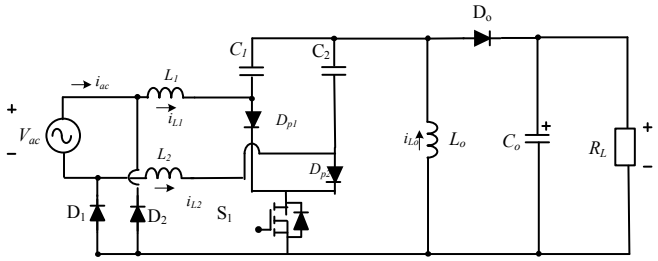


Fig. 1 Conventional single switch bridgeless PFC SEPIC rectifier [20]

In this case, this paper attempts to solve several issues from the existing bridgeless PFC SEPIC by selecting the issues i.e., *PF*, THD_i, circulating current and output voltage ripple by using two-switch thus requires additional components. The circulating current occurs when the current returning path during positive-half flow through the L_2 and during negative-half cycle, the current returning path flow through to the L_1. Input diodes D_1 and D_2 are used to block the current during current returning to the AC source. Thus, the circulating current can be eliminated and achieve low THD_i and high *PF*. Besides, the reduction of the output voltage ripple of this proposed structure is done by increasing the output capacitance.

II. IMPROVED TSBPC SEPIC STRUCTURE

A. *Operation Principle of Improved TSBPFC SEPIC Structure (proposed structure)*

Fig. 2 shows the improved two-switch bridgeless SEPIC PFC structure. The line diodes D_1 and D_2 are connected in series at the input inductors L_1 and L_2 and the slow-recovery diodes are needed for the line switching frequency which is f_{Line} = 50 Hz.

Therefore, owing to the circuit symmetry, it is adequate to evaluate the circuit during the input voltage at positive half-period. The proposed structure is operated when the switch (S_1 = on and S_2 = off), (S_1 = off and S_2 = off), and (S_1 = off and S_2 = on) and there is no current flow through the body diode of MOSFET S at low-frequency current during the turned-on and turned-off states. The steady state operation during one switching period T_s can be divided in ten modes for current as shown Fig. 3, and it could be described as follows.

Mode 1: When the switch (S_1) is turned-on, and (S_2) is turned-off during the positive-half cycle, the energy from the AC source is stored at the input inductor (L_1), and the energy flow through to the (D_1) and (D_p). At the input inductor (L_2), small residual energy from the AC source flow through to the (D_2). During this interval, the parallel capacitor (C_p) is discharging, input capacitors (C_1 and C_2) and coupling capacitors (C_{c1} and C_{c2}) are in charging process. Thus, the output inductor (L_o) is charging. When the output diodes (D_o) is in blocking condition, the output capacitor (C_o) is discharging and the energy is transferred to the load, as shown in Fig. 4 (a).

Mode-2: Same condition with the Mode-1, only capacitors at the AC components are changed in this mode where the parallel capacitor (C_p) is charging while input capacitors (C_1 and C_2) and coupling capacitors (C_{c1} and C_{c2}) are discharging, as shown in Fig. 4 (a).

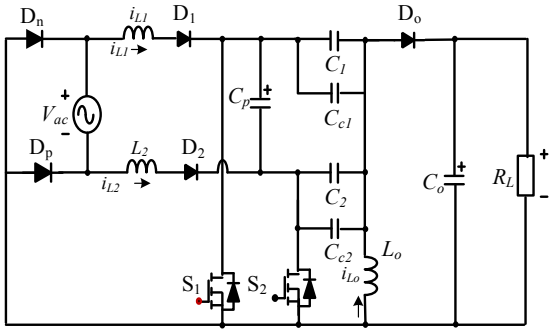
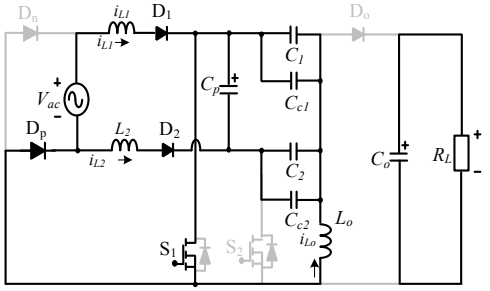
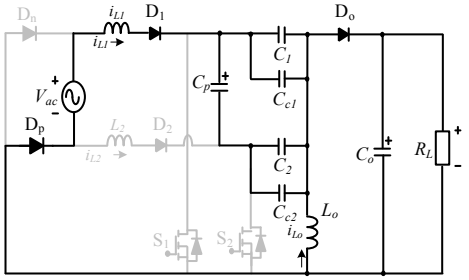


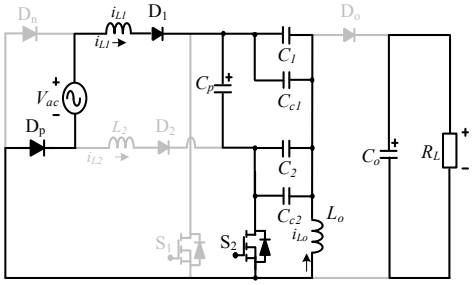
Fig. 2. Proposed two-switch bridgeless PFC SEPIC structure



(a)



(b)



(c)

Fig. 4. Mode of operation for two-switch PFC SEPIC structure (a) Mode 1 and Mode 2, positive-half cycle during S_1 t_{on}, (b) Mode-3, Mode-4, Mode-5, Mode-8, Mode-9, Mode-10, positive-half cycle during S_1 and S_2 t_{off}, and (c) Mode 6, and Mode 7, positive-half cycle during S_2 t_{on}

Mode-3: The input inductor (L_1) discharges during the turn-off of switch S_1 and S_2 and energy flow to the D_1 and D_p, while the input inductor (L_2) is not conducting as diode (D_2) are in off state. During this interval, the parallel capacitor C_p is charging. Input capacitor (C_1 and C_2) and coupling capacitor (C_{c1} and C_{c2}) are discharging. Besides, output capacitor (C_o) is discharging, and output diode (D_o) conducts

to the L_o, released the energy from AC source by looping condition as shown in Fig. 4 (b).

Mode-4: Same condition with the Mode-3, the output diode (D_o) is in blocking condition and the inductor input (L_1) and inductor output (L_o) are discharging. Meanwhile, the capacitor C_1, C_2 are charging, and then the current through inductor (L_1), and the input inductor (L_2) are discharging. The inductor output (L_o) and output capacitor (C_o) are charging, through the diode output (D_o) and the power is supplied to the load, as shown in Fig. 4 (b).

Mode-5: Same condition with Mode-4, the energy at the input inductor (L_1) is transferred to the input capacitor (C_1). Meanwhile, the output inductor (L_o) and output capacitor (C_o) are discharging through the output diode (D_o) and the power is supplied to the load as shown in Fig. 4 (b).

Mode-6: When the switch S_1 is turned off, and S_2 is turned on, the output inductor (L_1) is charging from the AC source. The input capacitors (C_1 and C_2) and coupling capacitors (C_{c1} and C_{c2}) discharges the energy to the output inductor (L_o). During this period, the output diode (D_o) is still in off state and the output capacitor (C_o) is discharged. Thus, the power from the output capacitor (C_o) is supplied to the load as shown in Fig. 4 (c).

Mode-7: Same condition with Mode-6, as shown in Fig. 4(c), the input inductor (L_1) stores energy from the AC source. At the same time, the output inductor (L_o) also stores energy by looping condition from AC source. The input capacitor (C_1 and C_2) and (C_{c1} and C_{c2}) are discharging. During this interval, the output diode (D_o) is turned off. The output capacitor C_o is discharging and the power is supplied to load as shown in Fig. 4 (c).

Mode-8: When the switch S_1 and S_2 are turned off, the input inductor (L_1) is discharging. During this interval, parallel capacitor (C_p) is discharging, while the input capacitor (C_1) and coupling capacitor (C_{c1}) are discharging, with C_2 and C_{c2} are charging. Meanwhile, the output inductor (L_o) and output capacitor (C_o) are discharging through the output diode (D_o) and the power is supplied to the load as shown in Fig. 4 (b).

Mode-9: Same condition with Mode-7, the input inductor (L_1) is discharging and the energy flow to the input diode (D_1) and D_p are conducting. During this interval, the parallel capacitor (C_p) is discharging. The input capacitor (C_1) and coupling (C_{c1}) are charging, besides C_2 and C_{c2} are discharging. The output inductor (L_o) and output capacitor C_o are discharging, and the output diode (D_o) is in forward bias, as shown in Fig. 4 (b).

Mode-10: Same condition with Mode-9 as shown in Figure 4(b), the input capacitor C_1 and C_2 store energy from input inductor (L_1). The coupling capacitor (C_{c1}) is charging, and C_{c2} is discharging. Meanwhile the output inductor (L_o) and output capacitor (C_o) are discharging thus the power is supplied to the load as depicted in Fig. 4 (c).

III. DESIGN CONSIDERATION

The consideration to design the converter is deliberated in this section, and specifications used are listed in Table 1.

TABLE I. SPECIFICATION OF THE PROPOSED CONVERTER

Parameter SEPIC	Values
RMS-Voltage AC Source, (V_{ac})	(50-100) V
Fundamental frequency, (f_L)	50 Hz
Switching frequency, (f_s)	50 kHz
Input inductors, (L_1 and L_2)	15.2 mH
Output inductor, (L_o)	25 µF
Input Capacitors, (C_1, C_{c1}, C_2, C_{c2})	1.5 µF,
Output Capacitor, (C_o)	3300 µF

A. Voltage Conversion Ratio

In order to calculate the input peak voltage and output voltage of TSBPFC SEPIC structure, the value of voltage conversion ratio (M) must be determined first:

$$M = \frac{V_o}{\sqrt{2}.V_{ac(rms)}} \tag{1}$$

The duty cycle can be expressed as a of function M as follows:

$$d_1 = \sqrt{\frac{KM}{\alpha}} \tag{2}$$

Where α and K are expressed as:

$$\alpha = -\frac{2}{\pi} - 2M - 1 + \frac{2M^2}{\pi\sqrt{M^2-1}}\left[\frac{\pi}{2} + \tan^{-1}\left(\frac{1}{\sqrt{M^2-1}}\right)\right] \tag{3}$$

$$K = \frac{2L_e}{T_s R_L} \tag{4}$$

Assuming the value of C_1 is equal to C_2, the capacitor coupling voltage is obtained based on the output voltage (V_o) and input voltage (V_i):

$$V_{c1} = \frac{V_o - V_{ac}}{2} \tag{5}$$

From (4), the average output current distribution during the switching cycle can be generated by calculating the value of equivalent inductor:

$$I_o = \frac{1}{4}\frac{d_1^2 V_{ac}^2}{fL_e V_{c1}} \tag{6}$$

From (5), the power balance principle between input and output power can be calculated as follows, assuming there are no losses occur:

$$V_{ac} I_{ac} = V_o I_o \tag{7}$$

Meanwhile, from (2), it can be determined that the TSBPFC SEPIC structure is operating in disconnected conduction mode (DCM) operation:

$$d_2 < 1 - d_1 \tag{8}$$

The principle of inductor is applied on the input inductors (L_1 and L_2), assuming to have the same duty cycle as follows:

$$d_2 = 1\frac{2\sin(\omega t)}{M - \sin(\omega t)} d_1 \tag{9}$$

B. Inductor Design in Bridgeless PFC SEPIC Structure

The value of inductor is calculated by considering the inductor ripple value is 10 % of the peak current:

$$\Delta i_{L1-\max} = 10\% i_{ac-peak} \tag{10}$$

From (9), the value of input inductor can be calculated as:

$$L_1 = \frac{1}{2}.\frac{V_{ac}(t)}{0.1 i_{ac-peak}}.\frac{d_1}{f_{sw}} \tag{11}$$

Based on (2), L_e can be formed by considering the input voltage AC (V_{ac}), output voltage (V_o), switching frequency (f_s) and current (I_{dc}), which is as follows:

$$L_e = \frac{(\sqrt{2}.V_{ac(rms)}.d_1)}{4.V_o.f_s.I_{dc}} \tag{12}$$

Therefore, the output inductor (L_o) can be obtained by using (11) and (12):

$$\frac{1}{L_o} = \frac{1}{L_e} - \frac{1}{L_1} - \frac{1}{L_2} \tag{13}$$

C. Capacitor Design in Bridgeless PFC SEPIC Structure

The energy in the coupling capacitor (C_1) and (C_2) will greatly influence the quality of the input line current. Thus, this coupling capacitor must be designed by using a constant voltage during the switching cycle, and frequency resonant must be much greater than the line frequency (f_L), so that there will be no oscillation at the input voltage at every line half cycle:

$$f < f_r < f_s \tag{14}$$

By assuming the capacitance of input coupling capacitor C_1 is equal to C_2, the magnitude of the resonance frequency is:

$$f_r = \frac{1}{2\pi\sqrt{(L_1 + L_o)(C_1 + C_o)}} \tag{15}$$

Where value of C_o is based on to the ripple voltage output. In this structure, the output ripple is set to be 3 % of the output voltage:

$$\Delta v_o = 3\%.V_o \tag{16}$$

Based on the (15), the output capacitance can be calculated as follows:

$$C_o = \frac{1}{0.03V_o}\left(\frac{d_1^2(\sqrt{2}V_{ac(rms)})^2}{4L_eV_{c1}}\left(\frac{1}{8f} + \frac{1}{4\pi f}\right) - \frac{V_o}{4fR_L}\right) \tag{17}$$

and the voltage capacitor coupling can be determined as follows:

$$V_{c1} = \frac{V_o - \sqrt{2}V_{ac(rms)}}{2} \tag{18}$$

The current value of parallel capacitor is the difference between the current at the input inductor and the current passing through the MOSFET:

$$I_{cn} = I_{L1} - I_{ds} \tag{19}$$

IV. Result and Analysis

A-100 W designed converter experimental listed in Table I before. An Altera FPGA is used to control the improved TSBPFC SEPIC structure. The experimental results are confirmed and agree well with the designed parameters.

A. Elimination of Circulating Current

Fig. 5 illustrates the experimental results for both structures i.e., existing structure and improve structure. The waveform shows that the circulating current is eliminated in the improved structure, which matches very well with the theoretical analysis. Fig. 5 (a) shows the results of the existing structure which consists of circulating current at the input inductors L_1 during negative-half cycle. It can be seen that, when the input inductor L_1 operates in positive-half cycle, the peak current of the input inductor $I_{L1(peak)}$ is 3.72 A. Meanwhile, during the negative half-cycle, the circulating current is 0.4 A with the AC current source of peak-to-peak is 8 A and AC voltage source of peak-to-peak is 140 V. Compared with the Fig. 5 (b), the circulating current is eliminated. The input inductors $I_{L1(peak)}$ is 2.6 A and $I_{L2(peak)}$ is 2.3 A for both cycles. The AC voltage source of peak-to-peak is 140 V and the AC current source is not measured due to the limitation of current prob. The experimental verification shows that the improved structure can eliminate the circulating current significantly.

B. Total Harmonic Distortion of Current Reduction

By using power analyzer, value of THD_i is measured and data is collected. In addition, an output capacitance of 3300 µF and fixed f_{sw} of 50 kHz are used for both structures. Fig. 6 (a) shows the AC current source of peak-to-peak is 8 A and AC voltage source of peak-to-peak is 140 V. The current THD of L_o = 22 µH is following the IEC 61000-3-2 standard with THD_i = 4.7% and the power factor is 0.98. The output voltage is 48 V and the output voltage ripple is 6 V. The output current is 2 A and the output current ripple is 0.5 A. When using various capacitance of output capacitors, the ripple of the output voltage at the waveforms is affected and consequently the parasitic element in components cause the spikes of the

output voltage waveform to be distorted. Fig. 6 (b) show the AC current source of peak-to-peak is 6 A and AC voltage source of peak-to-peak is 140 V. When the 3rd and 5th highest harmonics supressed as low as possible THD_i = 0.99% with the power factor is 0.98. Besides, the output voltage is 48 V and the output voltage ripple is 2.5 V while, the output current is 2.6 A and output current ripple is 0.4 A, proving that the experimental results agreed well with theoretical analysis when the parallel capacitors coupling are used.

V. CONCLUSSION

This paper presents an improve TSBPFC SEPIC structure for the THDi reduction and circulating current minimization. The current THD_i has been reduced 0.99% with the *PF* is 0.98. The current THDi requirement according to IEC 61000-3-2 standard should be less than 5% has been achieved. Besides, the circulating current is eliminated by using diodes D_1 and D_2, at the end of input inductor (L_1,L_2). The power output of this structure is increased by reducing circulating current. This topology uses the bridgeless SEPIC structure with two-switch (MOSFET)..

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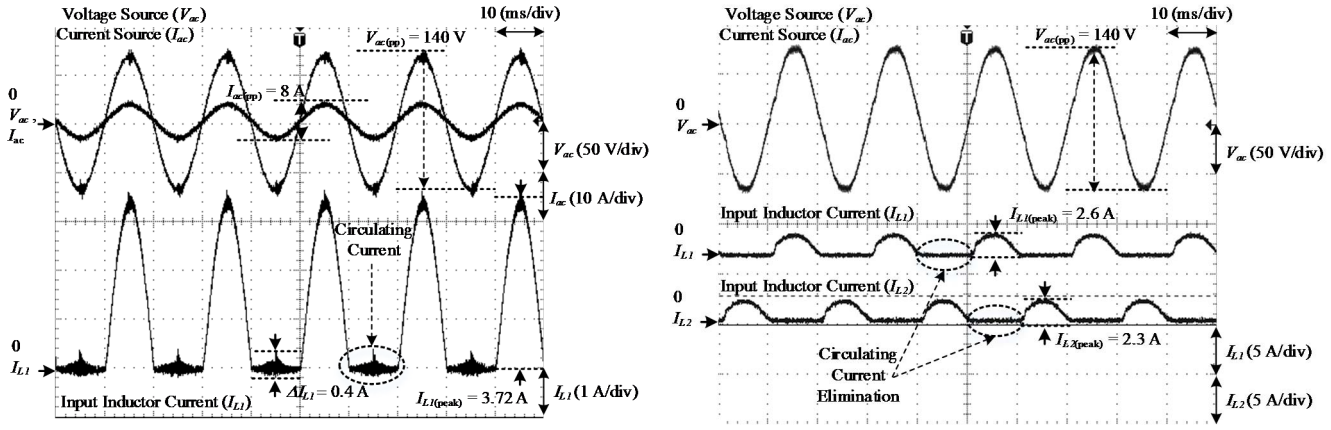

Fig. 5 Comparison of input inductor current (a) existing bridgeless PFC SEPIC (b) improve TSBPFC SEPIC

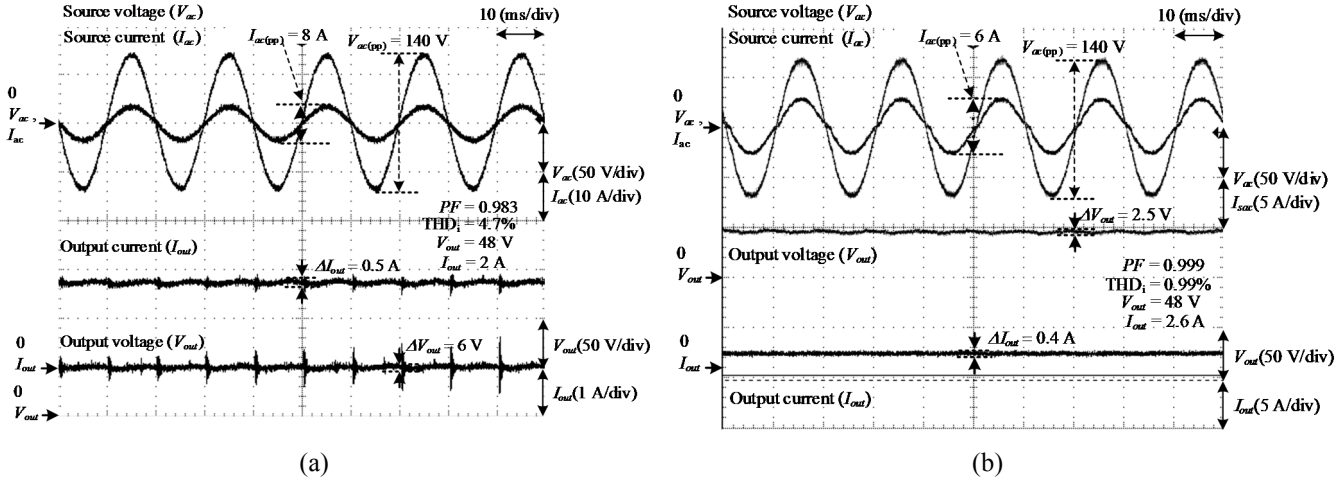

Fig. 6 Comparison of input and output AC source (a) existing bridgeless PFC SEPIC (b) improve TSBPFC SEPIC

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